DUAL GATE STRUCTURE FOR A FET AND METHOD FOR FABRICATING SAME

ABSTRACT OF THE DISCLOSURE

A method for fabricating a dual gate structure for JFETs and MESFETs and the associated devices. Trenches are etched in a semiconductor substrate for fabrication of a gate structure for a JFET or MESFET. A sidewall spacer may be formed on the walls of the trenches to adjust the lateral dimension for a first gate. Following the formation of the first gate by implantation or deposition, a buffer region is implanted below the first gate using a complementary dopant and a second sidewall spacer with a thickness that may be the same or greater than the thickness of the first sidewall spacer. Subsequent to the buffer implant, a second gate is implanted beneath the buffer layer using a third sidewall spacer with a greater thickness than the first sidewall spacer.